X-BAND Si BIPOLAR TRANSISTOR SINGLE-CHIP TRANSCEIVER USING THREE-DIMENSIONAL MMIC TECHNOLOGY

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ABSTRACT

The three-dimensional (3-D) MMIC technology significantly improves the operating frequency of Si MMICs and offers highly integrated masterslice MMICs. This paper introduces a newly developed X-band Si bipolar transistor transceiver MMIC which integrates 13 function blocks on a 2.3 × 2.3 mm chip; it offers 20 dB receiver gain and 13 dB transmitter gain. Its design uses a novel function-block-library concept based on the 3-D masterslice MMIC technology.

INTRODUCTION

Recent advances in wireless technology and its application to a variety of systems, such as cellular phones, satellite communications, and wireless LANs, have pushed the development of low-cost, high-speed, and low-power consumption multifunctional MMICs. Si MMICs have great advantages over GaAs MMICs such as a well-established fabrication process, lower process cost, and the potential for easy integration with digital LSIs. Several recent approaches have successfully implemented Si MMICs in wireless access applications. However, the operating frequency of the Si MMICs still remains several GHz. We have been proposing a three-dimensional (3-D) MMIC technology to overcome this problem. The 3-D MMIC technology greatly improves the operating frequency of Si MMICs [1][2] and offers highly integrated masterslice MMICs [3].

This paper describes a newly developed X-band transceiver MMIC. It integrates a 4-stage front-end amplifier and an image-rejection mixer for receiver operation, a balanced upconverter and an RF buffer amplifier for transmitter operation, and an LO buffer amplifier with switching function on a 2.3 × 2.3 mm chip; it offers 20 dB receiver gain and 13 dB transmitter gain. The first X-band operation of a Si-bipolar transistor T/R MMIC with very high integration level has been achieved using Si-based 3-D MMIC technology. A novel function-block-library concept based on 3-D masterslice MMIC technology is adopted in designing the transceiver. The concept effectively reduces the MMIC development turn-around-time (TAT) due to the reuse of well-established circuits.

STRUCTURE

The basic structure of the Si-based 3-D MMIC is shown in Fig. 1. Transistors, resistors, and lower electrodes of MIM capacitors are formed on a Si substrate and passivated. The second-level metal (Al) is formed on the

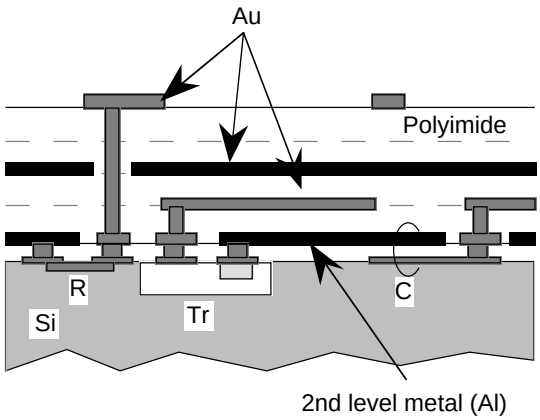

Fig. 1 Basic structure of Si-based 3-D MMIC.

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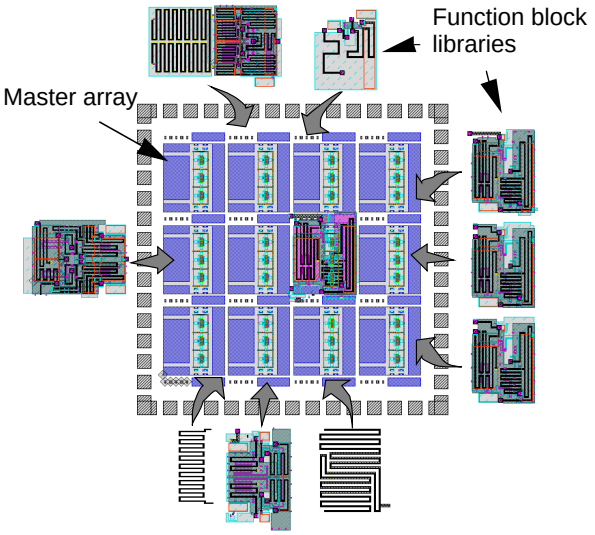


Fig. 2 Master array and function block libraries.

passivation film and selectively covers most of the wafer surface. The devices and the metals are formed using an ordinary Si IC process. After that, a 3-D passive structure constructed with four layers of 2.5-µm-thick polyimide films and four layers of 1-µm-thick Au metals (top metal is 2 µm thick) is formed on the second-level metal. The most significant feature of this structure is that the second-level metal electrically separates the substrate and 3-D passive structure. By using the second-level metal as a ground plane, the conductive loss of the Si substrate is effectively isolated from the 3-D passive circuits and we can obtain high-Q passive elements on Si substrates. As a result, the operating frequency of Si MMICs can be greatly improved using the reactive matching technique and these high-Q passive elements [1]. This structure also offers highly integrated masterslice MMICs.

FUNCTION BLOCK LIBRARY CONCEPT

The 3-D masterslice MMIC is a semi-custom MMIC similar to gate-array LSIs. It is constructed with a master array which includes many transistors, resistors, and lower electrodes of MIM capacitors arranged in a matrix and 3-D passive circuits created on the master array shown in Fig. 2. Unused devices and shunt capacitors are covered by the ground metal, which creates enough space for 3-D transmission lines. By using this technology, many kinds of circuits, i.e. function blocks, can be designed and laid out on the same footprint. Since each function block

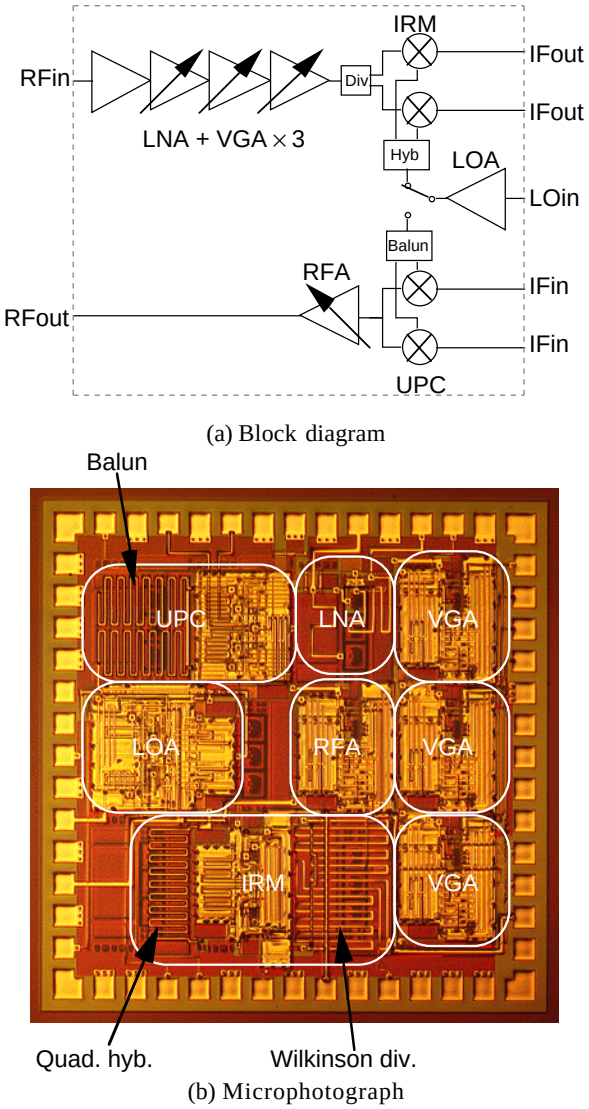
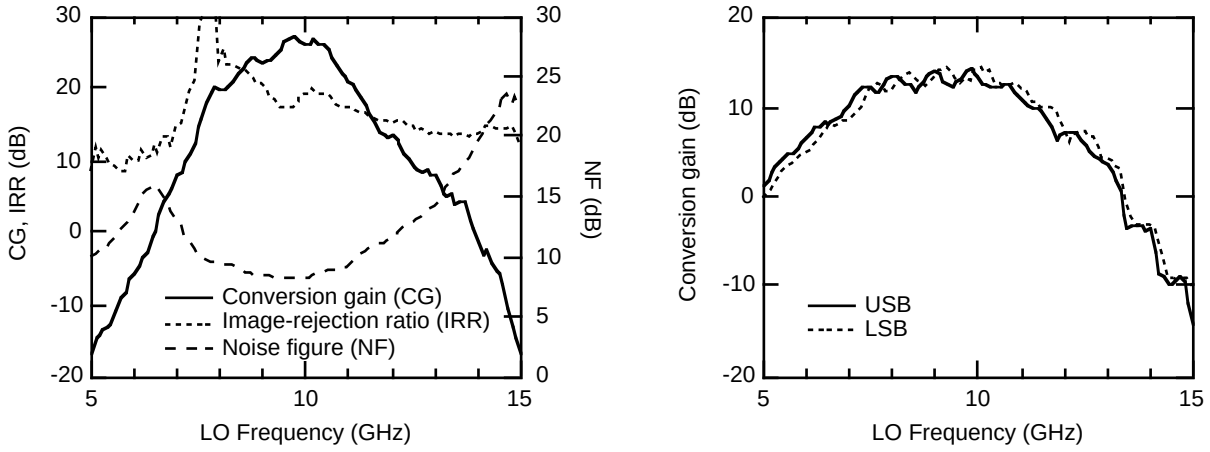


Fig. 3 Fabricated X-band single-chip tranceiver which includes a low-noise amplifier (LNA), three variable-gain amplifiers (VGA), an image-rejection mixer (IRM), a balanced upconverter (UPC), an RF buffer amplifier (RFA), and an LO buffer amplifier with switching function (LOA).

uses the same footprint and occupies very small area on the master array, it is easy to build a function block library. The library allows us to integrate a multifunctional MMIC, as well as evaluate each function block, in a very short TAT.

CIRCUIT DESIGN & PERFORMANCE

Figure 3 shows a block diagram and a microphotograph of the fabricated X-band single-chip transceiver MMIC



(a) Receiver mode

(b) Transmitter mode

Fig. 4 Measured performance of the fabricated X-band single-chip tranceiver.

using Si bipolar transistors (SST1C [4]). A 4-stage front-end amplifier and an image-rejection mixer for a receiver, a balanced upconverter and an RF buffer amplifier for a transmitter, and LO buffer amplifier with switching function are integrated on the 2.3 × 2.3 mm chip.

The front-end amplifier is constructed with a common-emitter BJT low-noise amplifier (LNA) and three cascode BJT variable-gain amplifiers (VGA). The LNA employs wide thin-film microstrip (TFMS) lines, which are constructed with signal lines located on top of the polyimide film and a second-level metal ground plane, to reduce the noise figure. In the VGA design, a ground plane is located in a middle of the polyimide layers and input- and output-matching elements are stacked above and below the ground plane to reduce the circuit area. Better than 30 dB gain and better than 8.5 dB noise figure are obtained at around 10 GHz.

The image-rejection mixer is constructed with two unit mixers, a quadrature hybrid, and a Wilkinson divider. The unit mixers employ the collector-LO-injection configuration and stacked structure similar to the VGA. The quadrature hybrid and the Wilkinson divider employ a 3-D broad-side coupler and TFMS lines, respectively. They are folded into meander-like configurations as shown in the microphotograph. Conversion loss and image-rejection ratio are better than 10 dB and 15 dB, respectively, at around 10 GHz.

The upconverter is constructed with two base-LO-injection mixers and a balun. The balun is a Marchand balun that employs two 3-D broad-side couplers folded into meander-like configuration to reduce the circuit area. The RF buffer amplifier is the same as the VGA used in the front-end amplifier.

The LO amplifier is constructed with a common-emitter BJT followed by two parallel common-base BJTs. By changing the bias voltages of the common-base BJTs, the output LO power can be switched to either the image-rejection mixer or the upconverter. Better than 10 dB gain and 10 dBm output power are obtained.

Figure 4 shows measured performances of the fabricated X-band transceiver MMIC. Better than 20 dB gain and 15 dB image-rejection ratio are obtained from 8 to 11 GHz in receiver mode when the RF input power is -50 dBm. IIP3 is -25 dBm. Noise figure is around 8.5 dB. Conversion gain in the transmitter mode is around 13 dB. Saturated RF power is -7 dBm when LO frequency is 10 GHz and IF input power is -20 dBm. LO power is 0 dBm and IF frequency is 140 MHz.

CONCLUSION

The 3-D MMIC technology greatly improves the operating frequency of Si MMICs and makes them competitive with GaAs MMICs in terms of frequency band. It also offers highly integrated masterslice MMICs which are semi-custom MMICs similar to gate-array LSIs. This paper introduced a highly integrated X-band Si bipolar transistor transceiver MMIC using a novel function-block-library concept based on the 3-D masterslice MMIC technology. The Si 3-D MMICs using SiGe HBTs, CMOSs and BiCMOSs also have the potential to be easily

integrated with digital LSIs at low cost. This technology promises to achieve cost effective intelligent wireless communication equipment and goes a long way in supporting the forthcoming multimedia era.

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